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A Novel high performance Junctionless FinFET

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Abstract: The recent scaling down of CMOSFET 's poses challenge to industrial fabrication of ultra-shallow abrupt source-drain junction. Though FinFET, tri-gate MOSFET reduces short channel effects, all these devices might suffer from fabrication or reliability related issues. For example, the FinFET requires gate to be patterned across the fin. Three-dimensional devices also require doping to be conformal, increasing the complexity of junction formation, which, in any case, becomes more challenging with every new technology node.

The proposed Junction less FinFET device has no junctions, contains same doping gradients so they are thought to be simpler fabrication process, less variability and better electrical property than classical inversion mode devices. It was observed that the proposed device have stronger immunity against Short channel effect, because it has a longer effective channel length than the physical length. This structure has excellent electrostatic Integrity, improved drain induced barrier lowering and sub-threshold swing, reduced OFF state leakage current was observed. In this paper, both the forward and reverse characteristics JLFinFET with deep nano-scale design parameters have been studied.

Keywords: High performance Junctionless FinFET.

Introduction:

Large Scale Integrated circuits (LSI's) started in early1970's as memories[1] and microprocessors[2] using 10 µm p-channel MOSFETs, have evolved to 22 nm CMOS VLSI's (Very large Scale Integrated circuits) During the past 44 years, we have experienced 18 generations for the downsizing, contributing to the continuation of the Moore's law[3] . Every 2.5 years in average, the line width and area for a MOSFET decreases with factor of 0.7 and 0.5, respectively. As a result, the line width and area reduced by 450 and 200,000 times in 44 years. Not only the number of the MOSFETs in a single LSI chip increased, but also the performance - such as operational speed and power consumption per computational operation or function – of LSI's was enhanced dramatically because of decrease in capacitance and supply voltage.

The scaling of channel lengths in conventional metal oxide field effect transistor (FETs) shrinks to the order of nanometers leads to several critical challenges, such as the need to reduce short channel effect (SCE), to deliver a higher ON- current, to reduce power consumption, and to eliminate intrinsic parameter fluctuations must be addressed. Numerous approaches for addressing these issues have been introduced in past decade. These include the use of high-k/metal gate to suppress the direct tunnelling current in gate oxides, to enhance

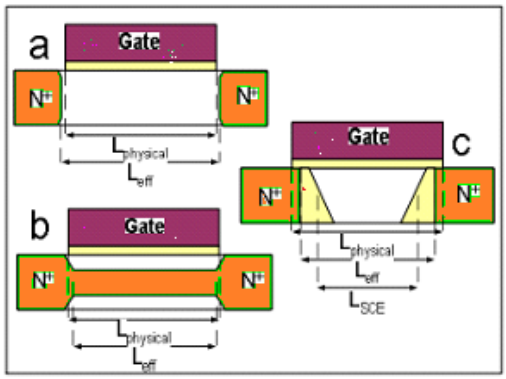
mobility using strain and to develop multi-gate structure such as FinFET and nanowire structures to reduce short channel effect.

Recently the concept of junctionless transistor which contains a single doping species at the same level in its source, drain and channel, is investigated. It is a promising metal – oxide – semiconductor field-effect transistor (MOSFET) architecture for continued scaling[1-5].

In MOSFET with junctions, part of the reduction of the threshold short-channel effects is due to the presence of a space-charge region associated with the junctions (SCE in equation below), and part of it (DIBL) is due to the growth of the drain space-charge region with drain voltage:

$V_{th} = V_{th\infty}$-SCE- DIBL

where $V_{th\infty}$ is the long-channel threshold voltage . In a MOSFET with physical gate length $L_{physical}$ the effective gate length is L_{eff} when the device is on, and the effective gate length is L_{SCE} when the device is off. Note that $L_{SCE} < L_{eff}$, which means that the "effective" channel length when the device is off is shorter than when it is on. In the junctionless transistor, the doping concentration is constant across the device. The electrostatic "squeezing" of the channel in the off device propagates into the source and drain; as a result, $L_{eff} > L_{physical}$ when the device is off 1a). When the device is on, the "squeezing" effect is removed, such that $L_{eff} = L_{physical}$ .As a result, L_{eff} is larger on the off state than in the on state, which improves short-channel effects.



The Junctionless device is basically a gated resistor, that is it is a resistor with a gate which control the carrier density and hence the current flow. The Junctionless device works like a low-resistance resistor, and the application of a gate voltage allows the semiconductor film of carriers to be depleted, thereby modulating its conductivity. Functionally, below the threshold voltage it is fully depleted and partially depleted when gate voltage reaches a Flat band voltage. As the channel is heavily doped the flat band voltage VFB is almost equal to V_{dd}.

The main advantages of JLT over its conventional counterpart are: 1) avoidance of the use of an ultra-shallow source/drain junction, which greatly simplifies the process flow, no need of ultra-steep doping gradients at source / drain, 2) low thermal budget for dopant activation that does not require annealing after gate stack formation and 3) superior short channel characteristics.

Introduction of high-k spacers can provide strong electric field coupling between gate and S/D extension region that reduces S/D resistance, on the other hand, spacers increase the fringe capacitance that degrades the circuit performance in terms of delay and access times in digital applications. With high-k spacers in extension regions can be electrically induce, which can reduce the SCEs. The use of high-k spacers for Junctionless can improve the electrostatic integrity of the device, resulting in lower OFF state leakage current, better short channel immunity and hence better scalability, simpler fabrication process, impact ionization induced steep sub-threshold slope at relatively lower drain bias than inversion mode , lower electric field in on-state etc. The Junctionless device is benefitted with an increase in high-k value in terms of better I_{ON}/I_{OFF} ratio, improved sub-threshold swing (SS) and DIBL effect.

This paper comprehensively investigates the device and circuit performances of Junctionless bulk FinFET by using 3-D quantum transport device simulation. This paper is structured as follows. In Section II, the simulation method and the setting of the parameters for studying the characteristics of devices and circuits are

introduced. In Section III, the performances of Junctionless device is presented. Finally, Section IV summarizes the conclusion.

II. TCAD Simulator

Silvaco TCAD simulator from SILVACO is used to perform all the simulations. The simulator has many modules and the following are used in this study.

- ATLAS: To create the device structure, to define doping, to define contacts, and to generate mesh for device simulation
- DeckBuild: To perform run time environment.
- Devedit :To create the device structure and mesh editor.
- Inspect and Tony Plot: To view the results.

The physics section of DEVEDIT includes the appropriate models for quantization of inversion layer charge, doping dependency of mobility, effect of high and normal electric fields on mobility, and velocity saturation.

Iii. Simulation Methodology:

Figure 2 shows the architecture of the junctionless FinFET used for simulation. The source, drain and the channel are uniformly heavily doped with $1.5e^{19}$ concentration. The source drain extension length is 15 nm. A single spacer material is used throughout the L_{ext} on both sides of gate from gate edge to S/D edges. For high K spacer materials SiO_2 and HfO_2 are considered in the paper .The effective channel length L_{eff} is 45nm and physical gate length(L_g) is 15nm are kept equal to make suitable analysis. The device dimensions and the electrical parameters are as follows.

Designing Constrains:

Parameters	Nominal Value
Gate Length	15 nm
Fin Width	10 nm
Source/drain width	10 nm
Source/drain length	10 nm
Gate oxide thickness	1 nm
Channel depth	10nm
Source/drain extensions	15nm

Junctionless 3-D structure:

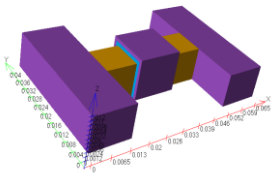


Figure.2 3-D JL structure

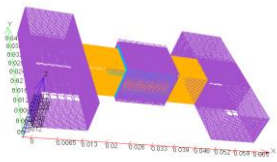


Figure.3 3-D meshed JLstructure

3-D structure with spacers:

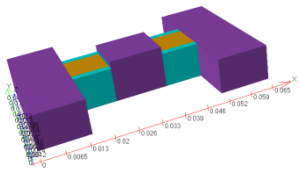


Figure.4:3-D JL structure with spacers

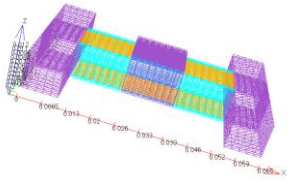


Figure.4:3-D meshed structure with spacers

Measurements:

Drain current vs. gate voltage is shown in Figure 3 for a 45nm device. The short-channel effects are very low. The sub-threshold slope (SS= dV_G / d(log(I_D)) at V_{DS}=1V is as low as 60 mV/dec for L=45 nm (Figure 4). The DIBL, defined as V_{TH} @ V_{ds}=50mV - V_{TH} @ V_{ds}=1V is equal to 7 mV for L=50 nm. These low values of DIB L are attributed to the absence of a drain junction. The blocking of current flow in the off state is not due to a reverse-biased drain junction but to "squeezing" off the carriers out of the channel region. When the device is off, the drain-source voltage drop occurs in the drain itself, and not in the channel region (under the gate) as in a regular device. This dramatically reduces DIBL. The lack of channel length modulation by the drain is also visible in the output characteristics which quite flat in saturation.

Results and Discussion

Gate Voltage versus drain current:

Figure 5 shows the graph between input gate voltage and drain current. The I-D current should increase linearly beyond the threshold voltage of the device with respect to the input gate voltage.

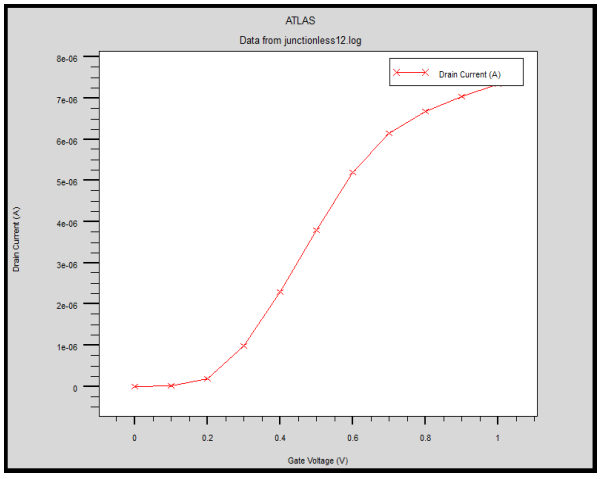


Figure.5:i-d curve

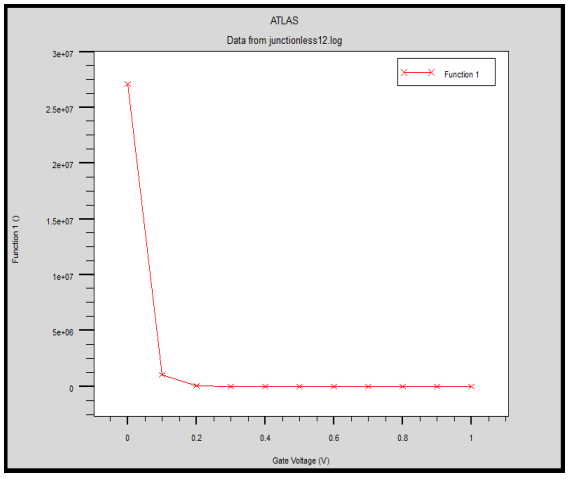


Figure.6: resistance curve

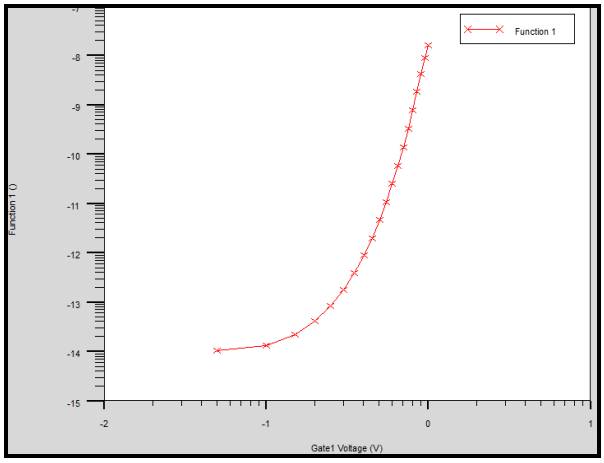


Figure.7 transconductance curve

Conclusion:

In this paper, we have designed the junctionless transistor with high permittivity spacers. Spacers in the extension regions enhance the controllability gate on the channel and effective gate length is increased that improve the electrostatic integrity of the device. The drain current, leakage current and their ratio is improved along with lower sub-threshold swing and reduced DIBL effect.

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